REMARKS

Claims 1-23 were previously pending. Applicant has withdrawn claims 11-17 from consideration in response to the Examiner's restriction requirement. Therefore, claims 1-10 and 18-23 are currently under consideration. The Examiner has rejected claims 1-10 and 18-23 under §103 in light of U.S. Patent No. 6,660,599 to Han et al., U.S. Patent No. 5,290,396 to Schoenborn et al., and U.S. Patent No. 6,362,105 to Moore. Applicants request consideration of the pending claims 1-10 and 18-23 in view of the following remarks and above amendments.

I. Claim Rejections – 35 U.S.C. §103

Claims 1, 18 and 21 are independent claims, each directed to a process to be applied to a semiconductor wafer. Claims 1, 18 and 21 all include applying a plasma etch process to a detection layer of a semiconductor wafer after the wafer has been planarized using a CMP process. Further, claims 1, 18 and 21 all include monitoring or looking for a signal that is generated from the plasma etching process. Specifically, claim 1, as amended, includes the step of "monitoring an optical signal during said plasma etching process, said optical signal being generated from the application of said plasma etching process to said detection layer." Claim 18 recites "applying a plasma etching process to a detection layer of material *until a signal is generated from said plasma etching process* that indicates that said detection layer has been removed from underlying features." (emphasis added). Finally, claim 21 recites "...applying a plasma etching process to a detection layer of material *until an identifiable signal is generated from said plasma etching process...*" The cited prior art references do not disclose monitoring or looking for a signal generated from the plasma etching process.

The Examiner primarily relied upon Han. However, Han does not disclose a method that includes monitoring an optical signal generated from the application of the plasma etching process to a detection layer (claim 1) or stopping the plasma etching process upon detection of a signal generated from the plasma etching process (claims 18 and 21). Han discloses the use of a polycrystalline silicon layer 114 used as a "blocking layer in the CMP process..." *See,* Han, col. 3, lines 44-46; col. 4, lines 19-21; col. 4, lines 32-37. Thus, Han teaches using the polycrystalline silicon "blocking layer" as a "shield" or layer of protection from the CMP process. Han then etches the "blocking layer" from the wafer. Han does not, however, teach monitoring or looking for any signal generated from applying the etching process to the "blocking layer." Further, with respect to claims 18 and 21, Han does not teach stopping the etching process upon detection of a signal generated during the etching process.

For at least the above-stated reasons, Applicant submits that independent claims 1-10 and 18-23 are allowable over the cited prior art.

CONCLUSION

Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 08-2025 in the name of Hewlett-Packard Company.

Respectfully submitted,

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